



# ***FM4442***

## ***256 Bytes Memory Card Chip***

Datasheet

---

Dec. 2008

INFORMATION IN THIS DOCUMENT IS INTENDED AS A REFERENCE TO ASSIST OUR CUSTOMERS IN THE SELECTION OF SHANGHAI FUDAN MICROELECTRONICS CO., LTD PRODUCT BEST SUITED TO THE CUSTOMER'S APPLICATION; THEY DO NOT CONVEY ANY LICENSE UNDER ANY INTELLECTUAL PROPERTY RIGHTS, OR ANY OTHER RIGHTS, BELONGING TO SHANGHAI FUDAN MICROELECTRONICS CO., LTD OR A THIRD PARTY. WHEN USING THE INFORMATION CONTAINED IN THIS DOCUMENTS, PLEASE BE SURE TO EVALUATE ALL INFORMATION AS A TOTAL SYSTEM BEFORE MAKING A FINAL DECISION ON THE APPLICABILITY OF THE INFORMATION AND PRODUCTS. SHANGHAI FUDAN MICROELECTRONICS CO., LTD ASSUMES NO RESPONSIBILITY FOR ANY DAMAGE, LIABILITY OR OTHER LOSS RESULTING FROM THE INFORMATION CONTAINED HEREIN. SHANGHAI FUDAN MICROELECTRONICS CO., LTD PRODUCTS ARE NOT INTENDED FOR USE IN MEDICAL, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS. THE PRIOR WRITTEN APPROVAL OF SHANGHAI FUDAN MICROELECTRONICS CO., LTD IS NECESSARY TO REPRINT OR REPRODUCE IN WHOLE OR IN PART THESE DOCUMENTS.

Future routine revisions will occur when appropriate, without notice. Contact Shanghai Fudan Microelectronics Co., Ltd sales office to obtain the latest specifications and before placing your product order. Please also pay attention to information published by Shanghai Fudan Microelectronics Co., Ltd by various means, including Shanghai Fudan Microelectronics Co., Ltd home page (<http://www.fmsh.com/>).

Please contact Shanghai Fudan Microelectronics Co., Ltd local sales office for the specification regarding the information in this documents or Shanghai Fudan Microelectronics Co., Ltd products.

#### Trademarks

Shanghai Fudan Microelectronics Co., Ltd name and logo, the “复旦” logo are trademarks or registered trademarks of Shanghai Fudan Microelectronics Co., Ltd or its subsidiaries in China.

Shanghai Fudan Microelectronics Co., Ltd, Printed in the China, All Rights Reserved.

# Product Overview

## Description

FM4442 is the memory card chip developed by Shanghai FM Co., Ltd. This chip has 256×8 Bits EEPROM with write protect function and programmable security code. With its contact configuration in accordance to ISO standard 7816 (synchronous transmission), FM4442 can be widely used in different types of IC memory cards.

## Features

- 256×8-bits EEPROM organization;
- Byte-wise addressing
- 32×1-bit organization of protection memory
- Irreversible byte-wise write protection of lowest 32 addresses (Byte 0 ... 31)
- Two-wire link protocol
- End of processing indicated at data output
- Answer-to-Reset acc. to ISO standard 7816-3
- Data retention for minimum of ten years
- Programming time 2.5 ms per byte for both erasing and writing
- Contact configuration and serial interface in accordance with ISO standard 7816 (Synchronous transmission)
- Data can only be changed after entry of the correct 3-byte programmable security code (security memory)
- Compatible SLE4442

## Pin Assignment

VCC	<b>C1</b>	<b>C6</b>	GND
RST	<b>C2</b>	<b>C5</b>	NC
CLK	<b>C3</b>	<b>C4</b>	I/O

## Pin Function

Pin	Symbol	Function
C1	VCC	Supply voltage 2.5V ~ 5V
C2	RST	Reset
C3	CLK	Clock input
C4	I/O	Bidirectional data line (open drain)
C5	NC	Not Connected
C6	GND	Ground

# Function Description

The FM4442 consists of 256 x 8 bits EEPROM main memory and a 32-bit protection memory with PROM functionality. The main memory is erased and written byte by byte. Each of the first 32 bytes can be irreversibly protected against data change by writing the corresponding bit in the protection memory. Each data byte in this address range is assigned to one bit of the protection memory and has the same address as the data byte in the main memory which it is assigned to. Once written the protection bit cannot be erased (PROM).

## Reset and Answer-to-Reset

Answer-to-Reset takes place according to ISO standard 7816-3 (ATR). The reset can be given at any time during operation. In the beginning, the address counter is set to zero together with a clock pulse and the first data bit (LSB) is output to I/O when RST is set from level H to level L. Under a continuous input of additional 31 clock pulses the contents of the first 4 EEPROM addresses is read out. The 33rd clock pulse switches I/O to high impedance Z and finishes the ATR procedure.

Answer-to-Reset	Byte1	Byte 2	Byte 3	Byte 4
(HEX)	DO <sub>7</sub> ...DO <sub>0</sub>	DO <sub>15</sub> ...DO <sub>8</sub>	DO <sub>23</sub> ...DO <sub>16</sub>	DO <sub>31</sub> ...DO <sub>24</sub>

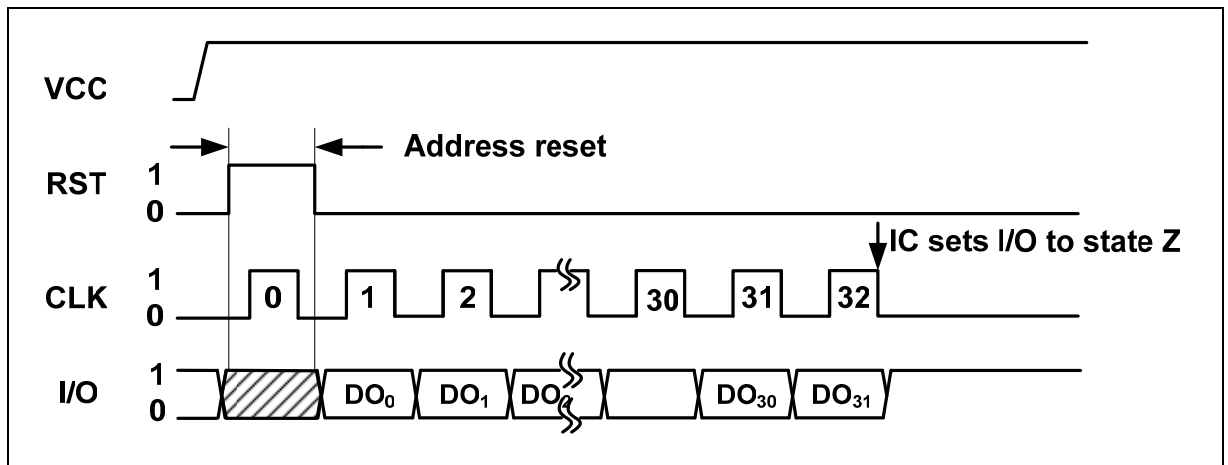


Figure 2 Reset and Answer-to-Reset

## Commands

Commands Format:

MSB				Control				LSB				MSB				Address				LSB				MSB				Data				LSB			
B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0								

### Command Introduction

#### (1) Read Main Memory

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7...A0	D7...D0
Binary	0	0	1	1	0	0	0	0	Address	No effect
Hexadecimal	30 <sub>H</sub>								00 <sub>H</sub> ...FF <sub>H</sub>	No effect

The command reads out the contents of the main memory (with LSB first) starting at the given byte address ( $N = 0 \dots 255$ ) up to the end of the memory. After the command entry the IFD has to supply sufficient clock pulses. The number of clocks is  $m = (256 - N) \times 8 + 1$ . The read access to the main memory is always possible.

#### (2) Read Protection Memory

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7...A0	D7...D0
Binary	0	0	1	1	0	1	0	0	No effect	No effect
Hexadecimal	34 <sub>H</sub>								No effect	No effect

The command transfers the protection bits under a continuous input of 32 clock pulses to the output. I/O is switched to high impedance Z by an additional pulse. The protection memory can always be read, and indicates the data bytes of the main memory protected against changing.

#### (3) Update Main Memory

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7...A0	D7...D0
Binary	0	0	1	1	1	0	0	0	Address	Input data
Hexadecimal	38 <sub>H</sub>								00 <sub>H</sub> ...FF <sub>H</sub>	Input data

The command programs the addressed EEPROM byte with the data byte transmitted. Depending on the old and new data, one of the following sequences will take place during the processing mode:

- erase and write (5 ms) corresponding to  $m = 245$  clock pulses
- write without erase (2.5 ms) corresponding to  $m = 124$  clock pulses
- erase without write (2.5 ms) corresponding to  $m = 124$  clock pulses

(All values at 50 kHz clock rate.)

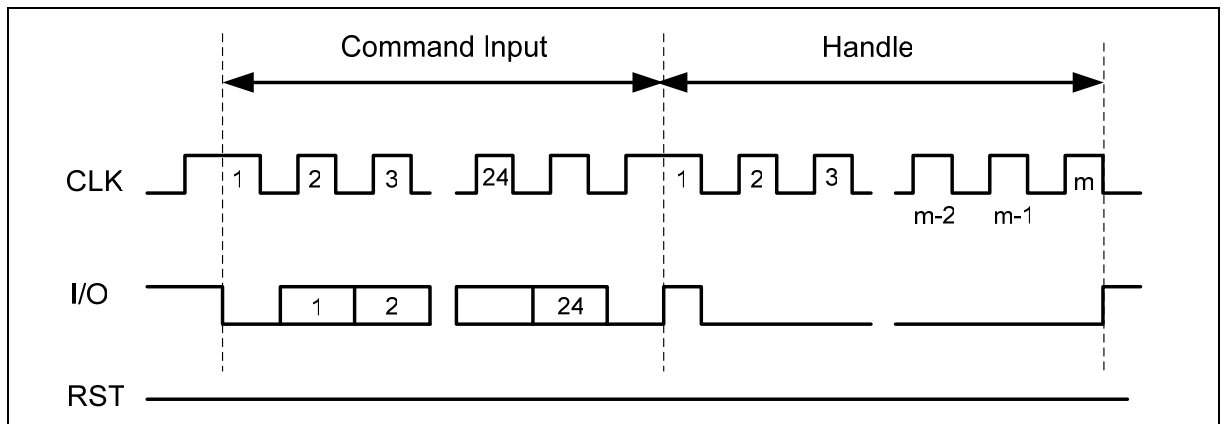


Figure 3 Update main memory

(4) Write Protection Memory

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7...A0	D7...D0
Binary	0	0	1	1	1	1	0	0	Address	Input data
Hexadecimal	3C <sub>H</sub>								00 <sub>H</sub> ...1F <sub>H</sub>	Input data

The execution of this command contains a comparison of the entered data byte with the assigned byte in the EEPROM. In case of identity the protection bit is written thus making the data information unchangeable. If the data comparison results in data differences writing of the protection bit will be suppressed.

(5) Read Security Memory

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7...A0	D7...D0
Binary	0	0	1	1	0	0	0	1	No effect	No effect
Hexadecimal	31 <sub>H</sub>								No effect	No effect

Similar to the read command for the protection memory this command reads out the 4 bytes of the security memory.

(6) Update Security Memory

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7...A0	D7...D0
Binary	0	0	1	1	1	0	0	1	Address	Input data
Hexadecimal	39 <sub>H</sub>								00 <sub>H</sub> ...1F <sub>H</sub>	Input data

Regarding the reference data bytes this command will only be executed if a PSC has been successfully verified before. Otherwise only each bit of the error counter (Address 0) can be written from "1" to "0". The execution times and the required clock pulses are the same as described under update main memory.

**(7) Compare Verification Data**

	Control								Address	Data
	B7	B6	B5	B4	B3	B2	B1	B0	A7...A0	D7...D0
Binary	0	0	1	1	0	0	1	1	Address	Input data
Hexadecimal	33 <sub>H</sub>								00 <sub>H</sub> ...03 <sub>H</sub>	Input data

The command compares one byte of the entered verification data byte with the corresponding reference data byte.

**PSC Verification**

The FM4442 requires a correct verification of the Programmable Security Code PSC stored in the Security Memory for altering data if desired. The following table gives an overview of the necessary commands for the PSC verification. The sequence of the shaded commands is mandatory.

Command	Control	Address	Data	Remark
	B7...B0	A7...A0	D7...D0	
Read security memory	31 <sub>H</sub>	No effect	No effect	Check error counter
Update security memory	39 <sub>H</sub>	00 <sub>H</sub>	Input data	Write free bit in error counter input data: 0000 0ddd binary
Compare verification data	33 <sub>H</sub>	01 <sub>H</sub>	Input data	Reference data byte1
Compare verification data	33 <sub>H</sub>	02 <sub>H</sub>	Input data	Reference data byte2
Compare verification data	33 <sub>H</sub>	03 <sub>H</sub>	Input data	Reference data byte3
Update security memory	39 <sub>H</sub>	00 <sub>H</sub>	FF <sub>H</sub>	Erase error counter
Read security memory	31 <sub>H</sub>	No effect	No effect	Check error counter

# Electrical Characteristics

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	$V_{CC}$	-0.3	-	6	V
Input voltage	$V_i$	-0.3	-	6	V
Storage temperature	$T_{sto}$	-25	-	+70	°C
Power dissipation	$P_{tot}$	-	-	70	mW

## Operation Range

Parameter	Symbol	Min.	Typ.	Max.	Unit
Ambient temperature	$T_A$	-20	-	+60	°C
Supply Voltage	$V_{CC}$	2.5	5.0	5.5	V

## DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply current	$I_{cc}$	-	3	10	mA
High level input voltage (I/O, CLK, RST)	$V_{ih}$	0.7 $V_{cc}$	-	$V_{cc}$	V
Low level input voltage (I/O, CLK, RST)	$V_{il}$	0	-	0.3* $V_{cc}$	V
High level input current (I/O, CLK, RST)	$I_h$	-	-	50	μA
Low level output current ( $V_{OL} = 0.4V$ , open drain)	$I_{ol}$	1	-	-	mA
High level output current ( $V_{OH} = 5V$ , open drain)	$I_{oh}$	-	-	50	μA
Input capacitance	$C_i$	-	-	10	pF

## AC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK Frequency $f_{CLK}$	$f_{CLK}$	7		50	kHz
I/O High time (Start Condition)	$t_1$	10			μs
CLK High to I/O Hold time	$t_2$	4			μs
I/O Low to CLK Hold time (Start Condition)	$t_3$	4			μs
I/O Setup to CLK High time	$t_4$	1			μs
CLK Low to I/O Hold time	$t_5$	1			μs
CLK High to I/O Clear time (Stop Condition)	$t_6$	4			μs
CLK Low to I/O Valid time	$t_7$			2.5	μs
CLK Low to I/O Valid time	$t_8$			2.5	μs
CLK Low to I/O Clear time	$t_9$			2.5	μs
RST High to CLK Setup time	$t_{10}$	4			μs
CLK Low to RST Hold time	$t_{11}$	4			μs
RST High time (address reset) time	$t_{12}$	20	50		μs
RST Low to I/O Valid time	$t_{13}$			2.5	μs
RST Low to CLK Setup time	$t_{14}$	4			μs



Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK High time	$t_{15}$	9			$\mu\text{s}$
CLK Low time	$t_{16}$	9			$\mu\text{s}$
CLK Low to I/O Valid time	$t_{17}$			2.5	$\mu\text{s}$
Reset time for Break	$t_{18}$	5			$\mu\text{s}$
RST High to I/O Clear time (Break)	$t_{19}$	2.5			$\mu\text{s}$
CLK Rise time	$t_R$			1	$\mu\text{s}$
CLK Fall time	$t_F$			1	$\mu\text{s}$
Erase time	$t_{ER}$	$2.5 @ f_{CLK} = 50\text{kHz}$			ms
Write time	$t_{WR}$	$2.5 @ f_{CLK} = 50\text{kHz}$			ms
Power on reset time				100	$\mu\text{s}$

### Timing Diagrams

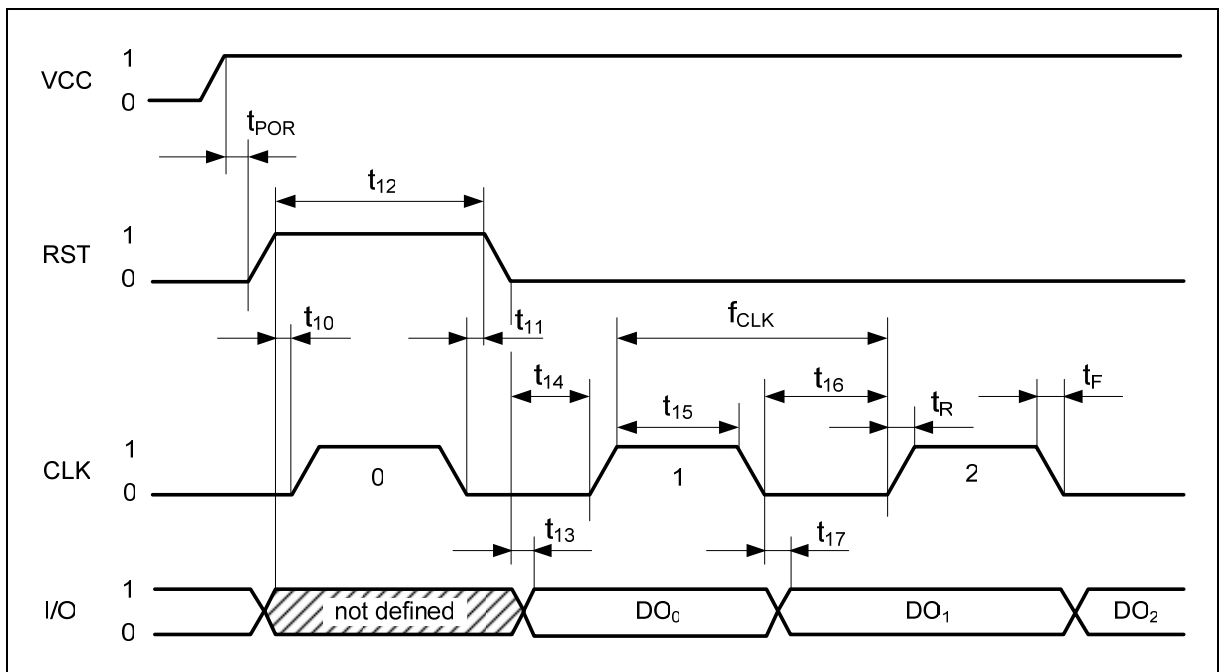


Figure 4 FM4442 Reset and Answer-to-Reset

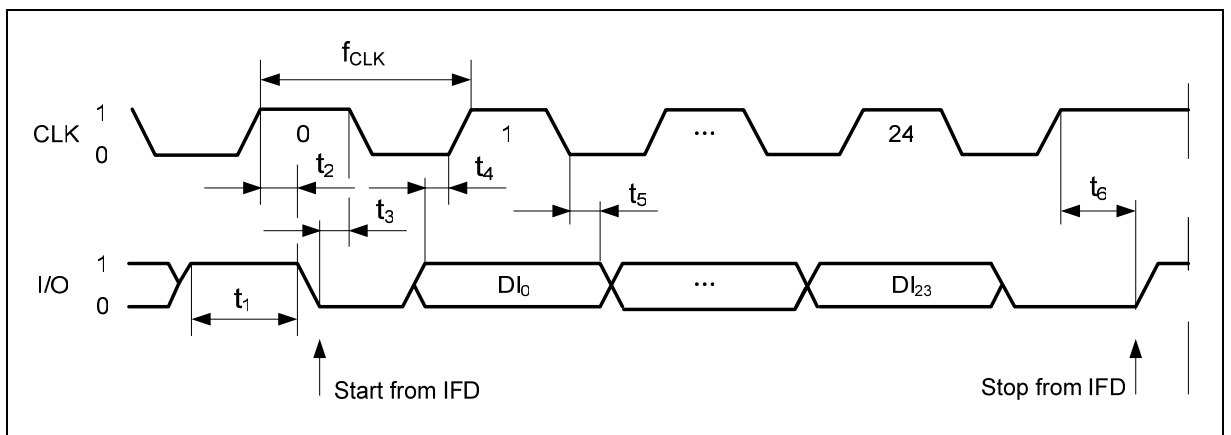


Figure 5 FM4442 Command Mode

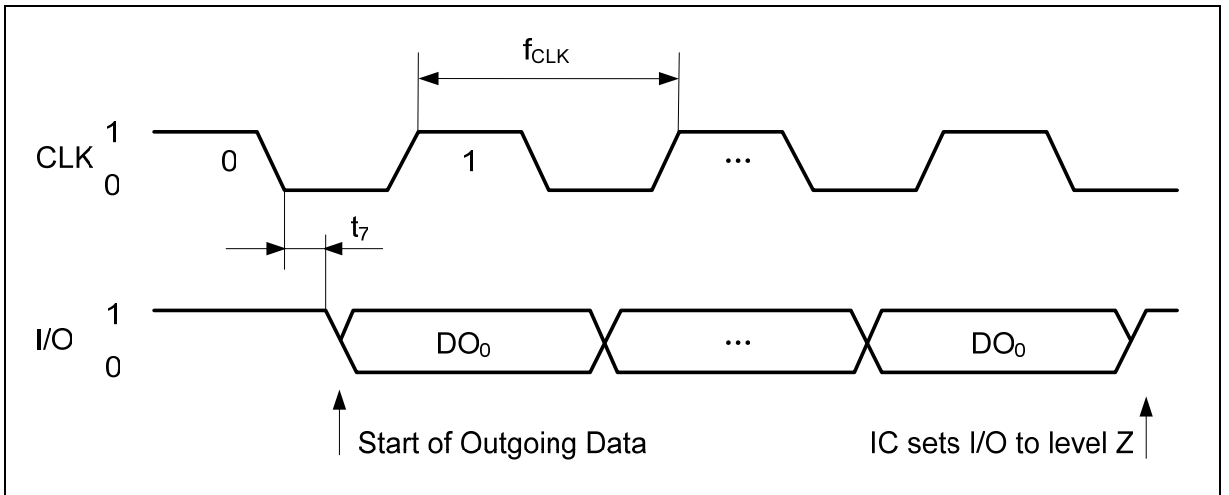


Figure 6 FM4442 Outgoing Data Mode

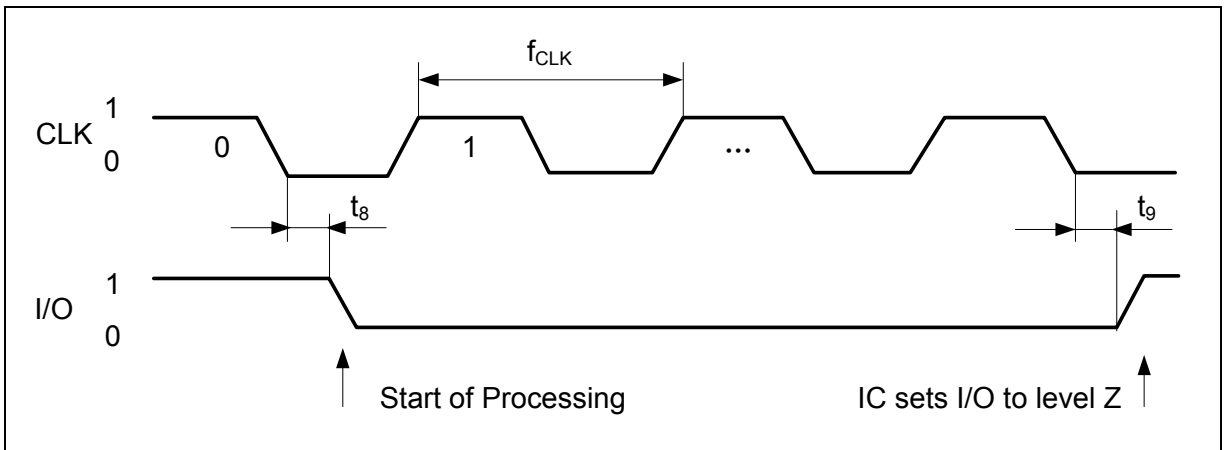


Figure 7 FM4442 Processing Mode

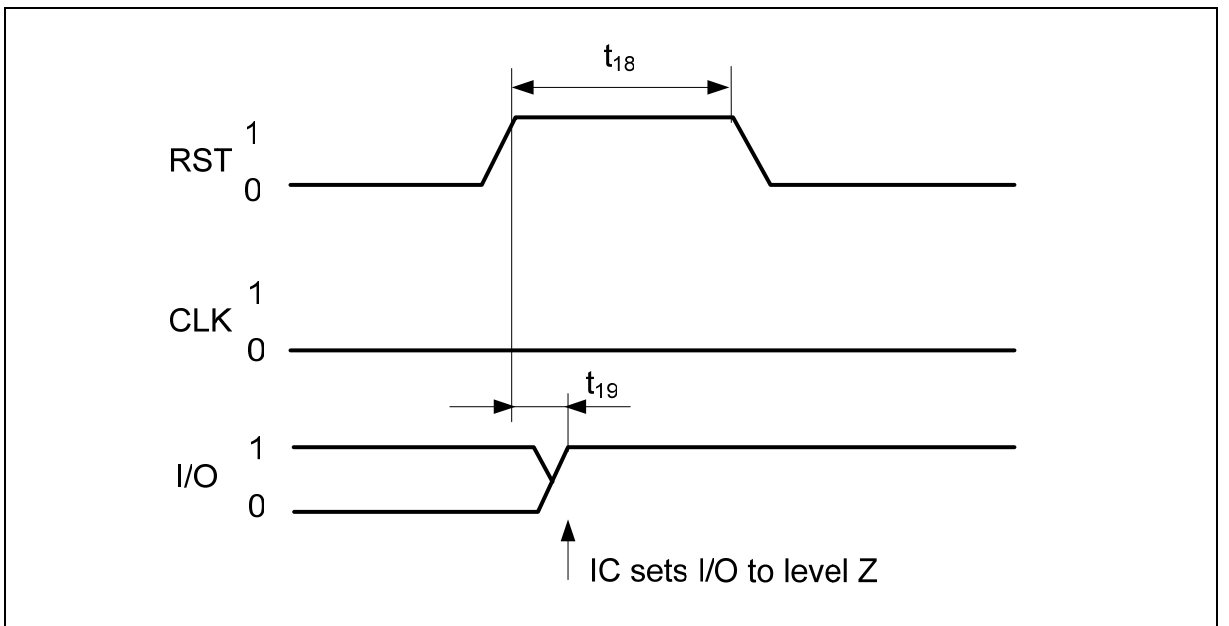


Figure 8 FM4442 Break

## Ordering Information

Ordering Code	Package	Product Carrier	Operation Range
FM4442-P5-R	Micro-Module Package (6Pin)	Reel	-20°C ~ +60°C
FM4442-M3-R	Micro-Module Package (6Pin)	Reel	

## Revision History

Version	Publication date	Pages	Paragraph or Illustration	Revise Description
1.0	Oct. 2007	10		Initial Release.
1.1	May. 2008	11	Sales and service	Updated the address of HK office.
2.0	Aug. 2008	13		Updated "Description"、"Electrical Characteristics" and "Ordering information".
3.0	Dec. 2008	13	Sales and service	Updated the address of Beijing office.

# Sales and Service

**Shanghai Fudan Microelectronics Co., Ltd.**

Address: Bldg No. 4, 127 Guotai Rd,  
Shanghai City China.

Postcode: 200433

Tel: (86-021) 6565 5050

Fax: (86-021) 6565 9115

**Shanghai Fudan Microelectronics (HK) Co., Ltd.**

Address: Unit 506, 5/F., East Ocean Centre, 98 Granville Road,  
Tsimshatsui East, Kowloon, Hong Kong

Tel: (852) 2116 3288 2116 3338

Fax: (852) 2116 0882

**Beijing Office**

Address: Room 419E, Bldg B, Gehua Building,  
1 QingLong Hutong, Dongzhimen Alley north Street,  
Dongcheng District, Beijing City, China.

Postcode: 100007

Tel: (86-10) 8418 6608 8418 7486

Fax: (86-10) 8418 6211

**Shenzhen Office**

Address: Room.1301, Century Bldg, Shengtingyuan Hotel,  
Huaqiang Rd (North),  
Shenzhen City, China.

Postcode: 518028

Tel: (86-0755) 8335 3211 8335 6511

Fax: (86-0755) 8335 9011

**Web Site:** <http://www.fmsh.com/>