IPJ-W1600

Monza® 5 Tag Chip Datasheet

Rev 1.51

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Overview

The Monza® 5 UHF RFID tag chip is optimized for serializing items such as apparel, electronics, cosmetics, documents and jewelry. It delivers unmatched read reliability for effective RFID business systems and record-breaking encoding performance to enable the lowest applied tag cost. The Monza 5 tag chip joins the Monza tag chip family, which is regarded as an industry leader in reliability, consistency, flexibility and Gen 2 & ISO-18000-6C compliance.

Features

- Superior read sensitivity of up to -20 dBm with a dipole antenna, combined with excellent interference rejection, delivers exceptional read reliability
- Industry leading write sensitivity of up to -16 dBm with a dipole antenna for unparalleled encoding reliability
- Industry-leading memory write speed enables encoding rates of over 3000 tags/minute and low applied tag cost
- Up to 128 bits of EPC memory with 32 bits of User memory
- 48 bits of Serialized TID
- EPCglobal and ISO 18000-63 compliant, Gen2V2 compliant.
- FastID™ mode enables 2x to 3x faster EPC+TID inventory for authentication and other TID-based applications
- TagFocus™ mode suppresses previously read tags to enable capture of more tags
- Scalable serialization built-in with Monza Self-Serialization
- Reduced manufacturing variability via a patent-pending repassivation later
- Extended temperature range (-40°C to +85°C) for reliability in harsh conditions
- Impinj's field-rewritable NVM, optimized for RFID, provides 100,000-cycle or 50-year retention reliability

Table of Contents

1 Introduction

1.1 Scope

This datasheet defines the physical and logical specifications for Gen 2-compliant Monza 5 tag silicon, a reader-talks-first, radio frequency identification (RFID) component operating in the UHF frequency range.

1.2 Reference Documents

EPC™ Radio Frequency Identity Protocols Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz, Version 1.2.0 (Gen 2 Specification). The conventions used in the Gen 2 Specification (normative references, terms and definitions, symbols, abbreviated terms, and notation) were adopted in the drafting of this Monza 5 Tag Chip Datasheet. Users of this datasheet should familiarize themselves with the Gen 2 Specification.

Impinj Monza Wafer Assembly Specification

Impinj Monza Wafer Map Orientation

EPC™ Tag Data Standards Specification

EPCglobal "Interoperability Test System for EPC Compliant Class-1 Generation-2 UHF RFID Devices" v.1.2.4, August 4, 2006. (Monza 5 tag chips are compliant with this Gen 2 interoperability standard.)

2 Functional Description

The Monza 5 tag chip fully supports all requirements of the Gen 2 specification as well as many optional commands and features (see Section 2.3 below). In addition, the Monza tag chip family provides a number of enhancements:

- Superior sensitivity for high read and write reliability
- Industry-leading memory write speed, delivering the highest encoding rates
- TagFocus™ inventory mode, a Gen 2 compliant method for capturing more hard-to-read tags by suppressing those that have already been read, by extending their S1 flag B-state
- FastID™ inventory mode, a Gen 2 compliant, patent-pending method for EPC+TID based inventory that is 2-3 times faster than previous methods
- A patent-pending "repassivation" spacing layer makes inlay manufacture less sensitive to die-attach pressure, resulting in less variance and more predictable performance in final inlay product (Monza 5 tag chips only)

2.1.1 Memory

Optimized for item-level tagging, Monza 5 tag chips offer EPC memory of up to 128 bits, serialized TID, and 32 bits of user memory. See Table 2-1.

Table 2-1 Monza 5 Memory Organization

Memory Section	Description
User	32 bits
TID (not changeable)	Serial Number—48 bits
	Extended TID Header—16 bits
	Company/Model Number—32 bits
EPC	Up to 128 bits
Reserved	Kill Password —32 bits
	Access Password – 32 bits

2.2 Advanced Monza Features Support More Effective Inventory

Monza tag chips support two unique, patent-pending features designed to boost inventory performance for traditional EPC and TID-based applications:

- TagFocus™ mode minimizes redundant reads of strong tags, allowing the reader to focus on weak tags that are typically the last to be found. Using TagFocus, readers can suppress previously read tags by indefinitely refreshing their S1 B state.
- FastID™ mode makes TID-based applications such as authentication practical by boosting TID-based inventory speeds by 2 to 3 times. Readers can inventory both the EPC and the TID without having to perform an access command. Setting the EPC word length to zero enables TID-only serialization.

2.3 Support for Optional Gen 2 Commands

Monza 5 tag chips support the optional commands listed in Table 2-2.

Table 2-2 Supported Optional Gen 2 Specification Commands

Command	Code	Length (bits)	Details
Access	11000110	56	
BlockWrite	11000111	>57	• Accepts valid one-word commands • Accepts valid two-word commands if pointer is an even value • Returns error code (00000000_2) if it receives a valid two-word command with an odd value pointer • Returns error code (00000000_2) if it receives a command for more than two words • Does not respond to block write commands of zero words

2.4 Monza 5 Tag Chip Block Diagram

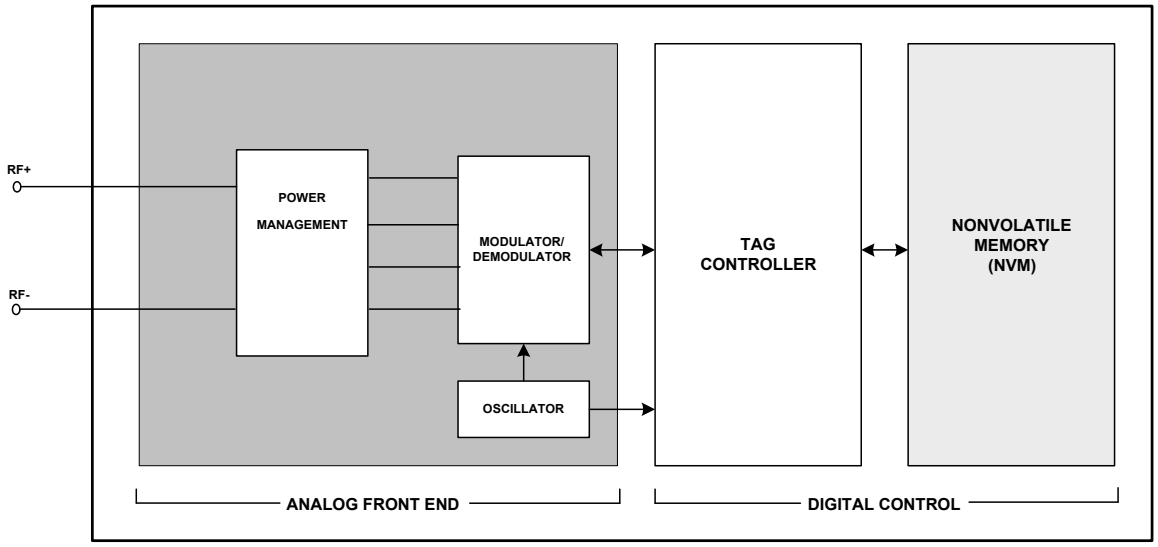

Figure 2-1 Block Diagram

2.5 Pad Descriptions

Monza 5 tag chips have four external pads available to the user: one RF+ pad, two RF- pads, and a non-connected pad designated NC. RF+ and RF- form a single differential antenna port. Table 2-3 (see also

Figure 2-1, and Figure 2-2). Note that none of these pads connects to the chip substrate.

Table 2-3 Pad Descriptions

External Signals	External Pad	Description
RF+	1	Differential RF Input Pads for Antenna. RF- has 2 pads to allow connection options. For details, see section 3.
RF-	2	

2.6 Differential Antenna Input

All interaction with the Monza 5 tag chip, including generation of its internal power, air interface, negotiation sequences, and command execution, occurs via its differential antenna port. The differential antenna port can be connected with an antenna in three different configurations (see Section 3.1).

1) RF+ and NC pads can be connected together on one terminal and the two RF- pads can be connected together on the second terminal.

2) RF+ pad can be connected on one terminal and the adjacent RF- pad can be connected on the second terminal.

3) RF+ and RF- pads can be connected diagonally with an antenna with the other pads (RF- and NC) left unconnected.

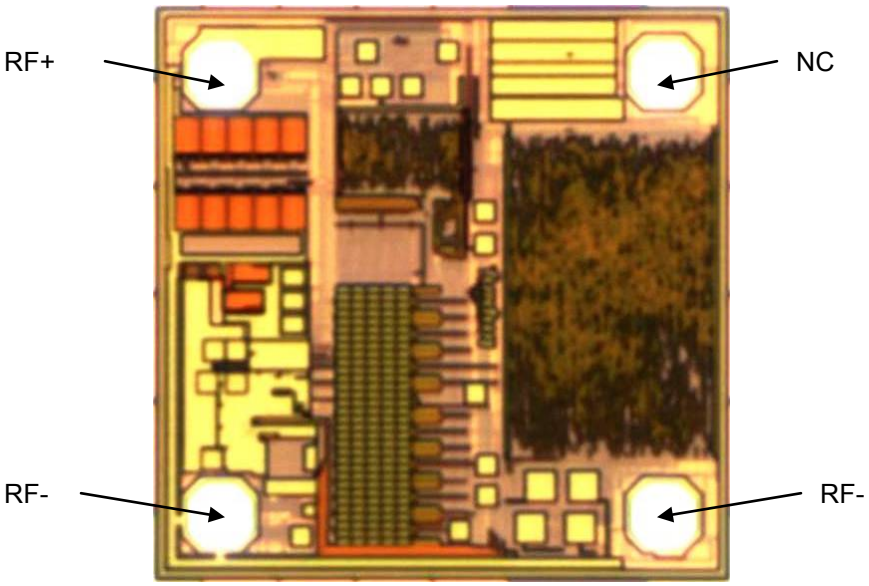

Figure 2-2 Monza 5 tag chip die orientation

2.7 Monza 5 Tag Chip Dimensions

Chip dimensions

- 465 µm x 465 µm square die size
- 70 µm bump top size
- 365 µm pad spacing
- 295 µm bump separation (inner edge to inner edge)

2.8 Power Management

The tag is activated by proximity to an active reader. When the tag enters a reader's RF field, the Power Management block converts the induced electromagnetic field to the DC voltage that powers the chip.

2.9 Modulator/Demodulator

The Monza 5 tag chip demodulates any of a reader's three possible modulation formats, DSB-ASK, SSB-ASK, or PR-ASK with PIE encoding. The tag communicates to a reader via backscatter of the incident RF waveform by switching the reflection coefficient of its antenna pair between reflective and absorptive states. Backscattered data is encoded as either FM0 or Miller subcarrier modulation (with the reader commanding both the encoding choice and the data rate).

2.10 Tag Controller

The Tag Controller block is a finite state machine (digital logic) that carries out command sequences and also performs a number of overhead duties.

2.11 Nonvolatile Memory

The Monza 5 tag chip embedded memory is nonvolatile memory (NVM) cell technology, specifically optimized for exceptionally high performance in RFID applications. All programming overhead circuitry is integrated on chip. Monza 5 tag chip NVM provides 100,000 cycle endurance and 50-year data retention.

The NVM block is organized into three segments:

- User memory with 32 bits
- EPC Memory with up to 128 bits
- Reserved Memory (which contains the Kill and Access passwords).

The ROM-based Tag Identification (TID) memory contains the EPCglobal class ID, the manufacturer identification, and the model number. It also contains an extended TID consisting of a 16-bit header and 48-bit serialization.

3 Interface Characteristics

This section describes the RF interface of the tag chip and the modulation characteristics of both communication links: reader-to-tag (Forward Link) and tag-to-reader (Reverse Link).

3.1 Making Connections

The pad arrangement of Monza 5 tag chips support three distinct configurations of connection to an antenna. The three connection options are illustrated in Figure -1, and described below.

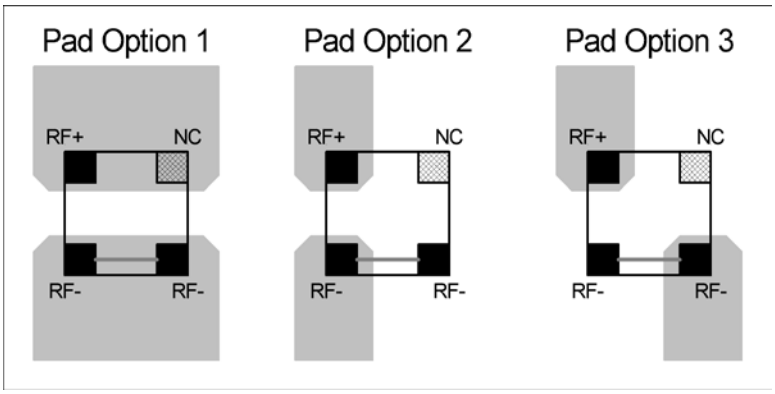

Figure 3-1: Antenna Connection Configuration Options

Connection option 1 contacts all four Monza 5 pads to the antenna, RF+ and NC to one terminal and the two RF- pads to the opposite polarity terminal. This option allows relatively coarse antenna geometry, and thus has the most relaxed requirements for antenna patterning resolution of the three options. Option 1 has the greatest chip-antenna overlap area of the three options, with a correspondingly higher parasitic mounting capacitance than either of the other two configurations.

Connection option 2 contacts just two pads, RF+ and the adjacent RF-. This option could be referred to as the "adjacent connection" or the "I" connection. The NC and unused RF- pads do not contact active antenna traces, but can mount to isolated antenna pads if desired, for example, for mechanical support. Option 2 has low chip-antenna overlap area, but it does place more stringent requirements on antenna patterning resolution and chip placement precision than Option 1.

Connection option 3 also contacts only two pads, RF+ and the opposite diagonal RF- pad. This "diagonal connection", also called the "X" connection, provides the greatest separation distance between the two antenna terminals out of the three configurations. It incurs a slight sensitivity penalty, approximately 0.3 dB, which is due to the additional length in the signal path across the chip compared to the adjacent connection of Option 2.

3.2 Impedance Parameters

In order to realize the full performance potential of the Monza 5 tag chip, it is imperative that the antenna present an appropriate impedance at its terminals. The nonlinear nature of the chip's power management circuits complicates the effort to find the optimum source impedance. Fortunately, it is possible to proceed with antenna design based on a linearized, lumped element model of the chip. The model, shown schematically in Figure 3-2, is a good mathematical fit for the chip over a broad frequency range. The lumped element values are listed in Table 3-1, where C_{mount} is the parasitic capacitance due to the antenna trace overlap with the chip surface, C_p appears at the chip terminals and is intrinsic to the chip, and R_p represents the energy conversion and energy absorption of the RF circuits.

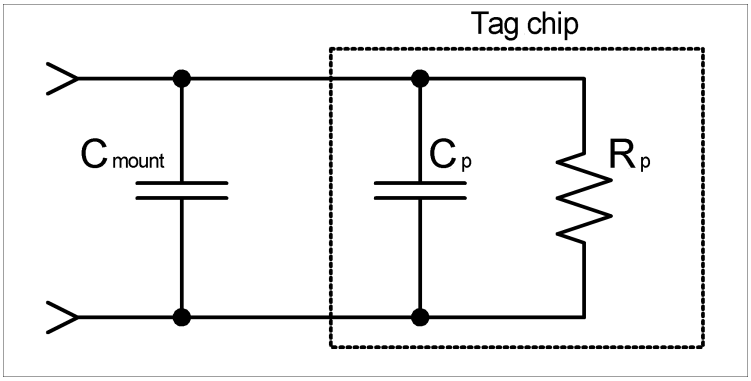

Figure 3-2: Tag Chip Linearized RF Model

Table 3-1 shows the values for the chip port model for the Monza 5 tag chip, which apply to all frequencies of the primary regions of operation (North America, Europe, and Japan).

Table 3-1 Chip Port Impedances

Parameter	Typical Value	Comments
C_p	0.825 pF	Intrinsic chip capacitance.
R_p	1.8 kOhm	
C_{mount}	0.245 pF	Typical capacitance due to adhesive and antenna mount parasitics. Total load capacitance presented to antenna is $C_p + C_{mount}$
Chip Read Sensitivity	-17.8 dBm	Measured at 25 °C; R=>T link using DSB-ASK modulation with 90% modulation depth, Tari=25 µs, and a T=>R link operating at 256 kbps with Miller M=4 encoding.
Chip Write Sensitivity	- 13.75 dBm	

3.3 Reader-to-Tag (Forward Link) Signal Characteristics

Table 3-2 Forward Link Signal Parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
RF Characteristics					
Carrier Frequency	860		960	MHz	North America: 902–928 MHz Europe: 865–868 MHz
Maximum RF Field Strength			+20	dBm	Received by a tag with dipole antenna while sitting on a maximum power reader antenna
Modulation		DSB-ASK, SSB-ASK, or PR-ASK			Double and single sideband amplitude shift keying; phase-reversal amplitude shift keying
Data Encoding		PIE			Pulse-interval encoding
Modulation Depth	80		100	%	(A-B)/A, A=envelope max., B=envelope min.
Ripple, Peak-to-Peak			5	%	Portion of A-B
Rise Time ($t_{r,10\text{-}90\%}$)	0		0.33Tari	sec	
Fall Time ($t_{f,10\text{-}90\%}$)	0		0.33Tari	sec	
Tari[1]	6.25		25	µs	Data 0 symbol period
PIE Symbol Ratio	1.5:1		2:1		Data 1 symbol duration relative to Data 0
Duty Cycle	48		82.3	%	Ratio of data symbol high time to total symbol time
Pulse Width	MAX(0.265Tari,2)		0.525Tari	µs	Pulse width defined as the low modulation time (50% amplitude)

3.4 Tag-to-Reader (Reverse Link) Signal Characteristics

Table 3-3 Reverse Link Signal Parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
Modulation Characteristics					
Modulation		ASK			FET Modulator
Data Encoding		Baseband FM0 or Miller Subcarrier			
Change in Modulator Reflection Coefficient $\|\Delta\Gamma\|$ due to Modulation		0.8			$\|\Delta\Gamma\| = \|\Gamma_{reflect} - \Gamma_{absorb}\|$ (per read/write sensitivity, Table 3-21)
Duty Cycle	45	50	55	%	
Symbol Period[1]	1.5625		25	µs	Baseband FM0
	3.125		200	µs	Miller-modulated subcarrier
Miller Subcarrier Frequency[1]	40		640	kHz	

Note 1: Values are nominal minimum and nominal maximum, and do not include frequency tolerance. Apply appropriate frequency tolerance to derive absolute periods and frequencies.

4 Tag Memory

4.1 Monza 5 Tag Chip Memory Map

Table 4-1 Physical/Logical Memory Map

Memory Bank Number	Memory Bank Name	Memory Bank Bit Address	Bit Number															
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
11_2	User	10_h-$1F_h$	User[15:0]															
		00_h-$0F_h$	User[31:16]															
10_2	TID (ROM)	50_h-$5F_h$	TID_Serial[15:0]															
		40_h-$4F_h$	TID_Serial[31:16]															
		30_h-$3F_h$	TID_Serial[47:32]															
		20_h-$2F_h$	Extended TID Header															
		10_h-$1F_h$	Manufacturer ID								Model Number							
		00_h-$0F_h$	1	1	1	0	0	0	1	0	Manufacturer ID							
01_2	EPC (NVM)	90_h-$9F_h$	EPC[15:0]															
		80_h-$8F_h$	EPC[31:16]															
		70_h-$7F_h$	EPC[47:32]															
		60_h-$6F_h$	EPC[63:48]															
		50_h-$5F_h$	EPC[79:64]															
		40_h-$4F_h$	EPC[95:80]															
		30_h-$3F_h$	EPC[111:96]															
		20_h-$2F_h$	EPC[127:112]															
		10_h-$1F_h$	Protocol-Control Bits (PC)															
		00_h-$0F_h$	CRC-16															
00_2	RESERVED (NVM)	30_h-$3F_h$	Access Password[15:0]															
		20_h-$2F_h$	Access Password[31:16]															
		10_h-$1F_h$	Kill Password[15:0]															
		00_h-$0F_h$	Kill Password[31:16]															

4.2 Logical vs. Physical Bit Identification

For the purposes of distinguishing most significant from least significant bits, a logical representation is used in this datasheet where MSBs correspond to large bit numbers and LSBs to small bit numbers. For example, Bit 15 is the logical MSB of a memory row in the memory map. Bit 0 is the LSB. A multi-bit word represented by WORD[N:0] is interpreted as MSB first when read from left to right. This convention should not be confused with the physical bit address indicated by the rows and column addresses in the memory map; the physical bit address describes the addressing used to access the memory.

4.3 Memory Banks

Described in the following sections are the contents of the NVM and ROM memory, and the parameters for their associated bit settings.

4.3.1 Reserved Memory

Reserved Memory contains the *Access* and *Kill* passwords.

4.3.2 Passwords

Monza 5 has a 32-bit Access Password and 32-bit Kill Password. The default password for both Kill and Access is $00000000_{h.}$

4.3.2.1 Access Password

The Access Password is a 32-bit value stored in Reserved Memory 20_h to $3F_h$ MSB first. The default value is all zeroes. Tags with a non-zero Access Password will require a reader to issue this password before transitioning to the secured state. A tag that does not implement an Access Password acts as though it had a zero-valued Access Password that is permanently read/write locked.

4.3.2.2 Kill Password

The Kill Password is a 32-bit value stored in Reserve Memory 00_h to $1F_{h,}$ MSB first. The default value is all zeroes. A reader shall use a tag's kill password once to kill the tag and render it silent thereafter. A tag will not execute a kill operation if its Kill Password is all zeroes. A tag that does not implement a Kill Password acts as though it had a zero-valued Kill Password that is permanently read/write locked.

4.3.3 EPC Memory (EPC data, Protocol Control Bits, and CRC16)

As per the Gen 2 specification, EPC memory contains a 16-bit cyclic-redundancy check word (CRC16) at memory addresses 00_h to $0F_h$, the 16 protocol-control bits (PC) at memory addresses 10_h to $1F_h$, and an EPC value beginning at address 20_h.

The protocol control fields include a five-bit EPC length, a one-bit user-memory indicator (UMI = 0), a one-bit extended protocol control indicator, and a nine-bit numbering system identifier (NSI). The factory-programmed value is 3000_h.

The tag calculates the CRC16 upon power-up over the stored PC bits and the EPC specified by the EPC length field in the stored PC. For more details about the PC field or the CRC16, see the Gen 2 specification.

A reader accesses EPC memory by setting MemBank = 01_2 in the appropriate command, and providing a memory address using the extensible-bit-vector (EBV) format. The CRC-16, PC, and EPC are stored MSB first (i.e., the EPC's MSB is stored in location 20_h).

The EPC memory bank of Monza 5 supports a maximum EPC size of 128 bits. The default configuration from the factory, however, is for a 96-bit EPC. It is possible to adjust the EPC size up or down from 96 bits, according to the parameters laid out in the Gen 2 standard. For Monza 5 chips (IPJ-W1600), the EPC value written into the chip

during factory test is listed below in Table 4-2. Care must be taken not to address EPC memory beyond word address 9.

Table 4-2 EPC at Manufacture

Impinj Part Number	EPC Value Pre-programmed at Manufacture (hex)
IPJ-W1600	3008 33B2 DDD9 0140 0000 0000

4.3.4 Tag Identification (TID) Memory

The ROM-based Tag Identification memory contains Impinj-specific data. The Impinj MDID (Manufacturer Identifier) for Monza 5 is 100000000001 (the location of the manufacturer ID is shown in the memory map tables above, and the bit details are given in Table). Note that a logic 1 in the most significant bit of the manufacturer ID (as in the example bordered in solid black in the table) indicates the presence of an extended TID consisting of a 16-bit header and a 48-bit serialization. The Monza 5 tag chip model number is located in the area bordered by the dashed line in TID memory row 10_h-$1F_h$ as shown in Table 3. The non-shaded bit locations in TID row 00_h-$0F_h$ store the EPCglobal™ Class ID (0xE2).

Table 4-3 TID Memory Details

Memory Bank Description	Memory Bank Bit Address	Bit Number															
10_2 TID (ROM)	50_h-$5F_h$	TID_SERIAL[15:0]															
	40_h-$4F_h$	TID_SERIAL[31:16]															
	30_h-$3F_h$	TID_SERIAL[47:32]															
	20_h-$2F_h$	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	10_h-$1F_h$	0	0	0	1	Monza 5 Model Number											
						0	0	0	1	0	0	1	1	0	0	0	0
	00_h-$0F_h$	1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0

4.3.5 User Memory

User memory contains two 16-bit words at memory addresses 00_h to $1F_h$ in memory bank 11_h.

5 Absolute Maximum Ratings

Stresses beyond those listed in this section may cause permanent damage to the tag. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this datasheet is not guaranteed or implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 Temperature

Several different temperature ranges will apply over unique operating and survival conditions. Table 5-1 lists the ranges that will be referred to in this specification. Tag functional and performance requirements are met over the operating range, unless otherwise specified.

Table 5-1 Temperature parameters

Parameter	Minimum	Typical	Maximum	Units	Comments
Extended Operating Temperature	–40		+85	°C	Default range for all functional and performance requirements
Storage Temperature	–40		+85	°C	
Assembly Survival Temperature			+150	°C	Applied for one minute
Temperature Rate of Change			4	°C / sec	During operation

5.2 Electrostatic Discharge (ESD) Tolerance

The tag is guaranteed to survive ESD as specified in Table 5-2.

Table 5-2 ESD Limits

Parameter	Minimum	Typical	Maximum	Units	Comments
ESD			2,000	V	HBM (Human Body Model)

5.3 NVM Use Model

Tag memory is designed to endure 100,000 write cycles or retain data for 50 years.

6 Ordering Information

Contact RFID_sales@impinj.com for ordering support.

Part Number	Form	Product	Processing Flow
IPJ-W1600-E00	Wafer	Monza 5 tag chip	Bumped, thinned (to ~100 µm), and diced

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